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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,553	09/15/2003	Yoichi Sato	03500.017560.	9044
5514	7590	09/12/2008	EXAMINER	
FITZPATRICK CELLA HARPER & SCINTO 30 ROCKEFELLER PLAZA NEW YORK, NY 10112		MCCOMMAS, BRENDAN N		
		ART UNIT		PAPER NUMBER
		2625		
		MAIL DATE		DELIVERY MODE
		09/12/2008		PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/661,553	SATO, YOICHI	
	<b>Examiner</b>	<b>Art Unit</b>	
	BRENDAN MCCOMMAS	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 20 May 2008.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-6 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 9/15/2003 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ .  | 6) <input type="checkbox"/> Other: _____ .                        |

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. **Claims 1-2, 4-5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Orava et al. (United States Patent 5,812,191) hereinafter referenced as Orava, further in view of Yamamoto et al. (United States Patent 7,098,950), hereinafter referenced as Yamamoto.

3. **Regarding claim 1**, Orava discloses a semiconductor high-energy radiation imaging device. In addition, Orava discloses an image pickup apparatus in which a pixel area, including a plurality of pixels each having a photoelectric conversion portion 20 and a common output portion 62 configured to sequentially amplify and output signals from the plurality of pixels included in the pixel area, is formed on a single semiconductor substrate, as disclosed in column 5, lines 39-50, column 16, lines 57-67 and exhibited in figure 4.

4. Regarding the common output portion, Orava discloses, in column 2 lines 27-35, that the semiconductor imaging device has an array of pixel cells including a semiconductor detector substrate and a semiconductor read out substrate, which are both integral to the semiconductor substrate, wherein:

5. The semiconductor readout substrate includes an array of individually addressable pixel circuits, each of which is connected to a corresponding pixel detector

cell to form a pixel cell, which reads on claimed, "common output portion for sequentially amplifying and outputting signals from the plurality of pixels included in said pixel area."

6. However Orava fails to explicitly disclose that the apparatus comprises:
7. a power supply unit configured to effect power supply control of the common output portion independently of control of the power supply to the pixel area; and
8. a control circuit configured to effect control to supply no power to the common output portion in a predetermined period after starting photo-charge accumulation in the photoelectric conversion portion and to supply power to the common output portion before the end of a photo-charge accumulation period in the photoelectric conversion portion.
9. However it would have been obvious to one of ordinary skill in the art at the time of the invention to include:
  10. a power supply unit configured to effect power supply control of the common output portion independently of control of the power supply to the pixel area; and
  11. a control circuit configured to effect control to supply no power to the common output portion in a predetermined period after starting photo-charge accumulation in the photoelectric conversion portion and to supply power to the common output portion before the end of a photo-charge accumulation period in the photoelectric conversion portion, as taught by Yamamoto.
12. In a similar field of endeavor, Yamamoto discloses an image sensor with stabilized black level and low power consumption. In addition Yamamoto discloses that the image sensor apparatus includes,

13. a power supply unit 21 configured to effect power supply control of the common output portion independently of control of the power supply to the pixel area, as disclosed in column 2, lines 32-46, column 7, lines 49-60 and exhibited in figure 11; and

14. a control circuit 22 configured to effect control to supply no power to the common output portion in a predetermined period after starting photo-charge accumulation in the photoelectric conversion portion and to supply power to the common output portion before the end of a photo-charge accumulation period in the photoelectric conversion portion as disclosed in column 8, lines 44-54, and exhibited in figure 11.

15. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include those modifications to the invention of Orava for the purpose of reducing power consumption.

16. **Regarding claim 2**, Orava and Yamamoto, the combination discloses everything claimed as applied above (see claim 1), in addition, Orava fails to explicitly disclose that the apparatus includes control circuitry which variably controls the period during which no power is supplied to the common output portion. However Yakamoto discloses the same in column 8, lines 44-54, and exhibited in figure 11.

17. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include this modification to the invention of Orava for the purpose of reducing power consumption.

18. **Regarding claim 4**, Orava and Yamamoto, the combination discloses everything claimed as applied above (see claim 1). In addition Orava discloses a semiconductor imaging device. Regarding the common output portion, Orava discloses, in column 2

lines 27-35, that the semiconductor imaging device has an array of pixel cells including a semiconductor detector substrate and a semiconductor read out substrate, which are both integral to the semiconductor substrate, wherein:

19. The semiconductor readout substrate includes an array of individually addressable pixel circuits, each of which is connected to a corresponding pixel detector cell to form a pixel cell, which reads on claimed, "common output portion for sequentially amplifying and outputting signals from the plurality of pixels included in said pixel area."

20. In addition Yamamoto discloses

21. a power supply unit 21 configured to supply a first power level (a first "reference voltage") and a second level lower than the first power level (0 or another "reference voltage") to the common output portion, as disclosed in column 2, lines 32-46, column 7, lines 49-60 and exhibited in figure 11

22. a control circuit 22 configured to effect control to supply power of the second power level to the common output portion in a predetermined period after starting photo-charge accumulation in the photoelectric conversion portion and supply the first power level to the common output portion before the end of a photo-charge accumulation period in the photoelectric conversion portion, as disclosed in column 8, lines 44-54, and exhibited in figures 11 and 12.

23. **Regarding claim 5**, Orava and Yamamoto, the combination discloses everything claimed as applied above (see claim 4), in addition, Orava fails to explicitly disclose that the apparatus includes control circuitry which variably controls the period during which

the second power level is supplied to the common output portion. However Yakamoto discloses the same in column 8, lines 44-54, and exhibited in figure 11.

24. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include this modification to the invention of Orava for the purpose of reducing power consumption.

25. **Claims 3 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Orava et al. (United States Patent 5,812,191) hereinafter referenced as Orava, further in view of Yamamoto et al. (United States Patent 7,098,950), hereinafter referenced as Yamamoto further in view of Kozuka et al. (United States Patent 6,163,024) hereinafter referenced as Kozuka.

26. **Regarding claim 3**, Orava and Takahashi, the combination discloses everything claimed as applied above (see claim 1), in addition, Orava and Takahashi fails to explicitly disclose that the apparatus wherein the power supply unit is formed on the single semiconductor substrate. However it would have been obvious to one of ordinary skill in the art at the time of the invention to include such a modification to the invention of Orava and Takahashi, as taught by Kozuka.

27. In a similar field of endeavor, Kozuka discloses a photoelectric transducer. In addition Kozuka discloses the apparatus wherein the power supply unit is formed on the single semiconductor substrate, as disclosed in claim 5.

28. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include this modification to the invention of Orava and Takahashi for the purpose of reducing noise in the image pickup process.

29. **Regarding claim 6**, Orava and Takahashi, the combination discloses everything claimed as applied above (see claim 4), in addition, Orava and Takahashi fails to explicitly disclose that the apparatus wherein the power supply unit is formed on the single semiconductor substrate. However it would have been obvious to one of ordinary skill in the art at the time of the invention to include such a modification to the invention of Orava and Takahashi, as taught by Kozuka.

30. In a similar field of endeavor, Kozuka discloses a photoelectric transducer. In addition Kozuka discloses the apparatus wherein the power supply unit is formed on the single semiconductor substrate, as disclosed in claim 5.

31. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include this modification to the invention of Orava and Takahashi for the purpose of reducing noise in the image pickup process.

#### ***Response to Arguments***

The arguments filed on 5/20/2008 have been fully considered but are not persuasive. On page 7 of the Applicants arguments, the Applicant argues “There does not appear to be any reference in these passages to a power supply unit configured to effect power supply control of the common output portion independently of control of the power supply to a pixel area.” However the examiner respectfully disagrees and points to column 2, lines 32-46 and column 7, lines 49-60 where Yamamoto discloses that the power supply supplies power independently (or at different times regardless if one region is on or not) to the read out portion BL2 and the pixel area BL1. In addition on page 8 of the Applicant’s arguments, the Applicant argues “the Office Action cites

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column 8, lines 44-54 of the Yamamoto et al as showing the claimed control circuit of Claims 1 and Claim 4. But this passage is not understood to disclose or suggest a control circuit configured to effect control to supply no power to the common output portion in a predetermined period after starting photo charge accumulation in the photo electric conversion portion and to supply power to the common output portion before the end of a photo charge accumulation period in the photoelectric conversion portion." The examiner respectfully disagrees and points to column 7 lines 49-60, where Yamamoto et al. disclose that the power supply controls the two areas independently to clear up any misunderstanding. In addition column 8, lines 44-54 are meant to address the limitation of a read-out period where there is first no power in the output portion, and then before the end of the photo charge accumulation, the power is given to the read out portion (in this case BL2 is the signal which activates the read-out portion independently of the photo charge accumulation power, which is signal BL1).

### ***Conclusion***

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brendan N. McCommas whose telephone number is 571-270-3575. The examiner can normally be reached on M-F (alternate F off) 7:30 am -5 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jefferey Harold can be reached on 571-272-7519. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ Brendan N. MCCommas/  
Examiner, Art Unit 2625

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/B. M./  
Examiner, Art Unit 2625

/Twyler L. Haskins/  
Supervisory Patent Examiner, Art Unit 2625